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COMPARISON OF METHODS OF IMPLEMENTATION OF EQUIVALENT SHAPERS IN CODE CONVERTERS

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A comparative analysis of two ways to implement the equivalent shaper in code converters is performed. An algorithm for constructing tables of laws of operation of the main non-standard node (equivalent shaper) in code converters by the method of accumulating equivalents is considered and proposed. The formulas for determining the number of rows of equivalents are obtained. Parallel and sequential strategies for using transformation steps are considered. The analysis of tables of equivalent generators was carried out, for the construction of which lexico-graphic enumeration of all transformation steps was used. An algorithm for constructing tables of the laws of functioning of equivalent generators is formulated. An analytical expression is obtained for determining the number of rows in tables of the laws of functioning of equivalent generators in code converters with a parallel strategy of using conversion steps. The conducted research allows to speed up the stage of system design of code converters.

Keywords*: equivalent shaper, code converter, algorithm, analysis, method of accumulation of equivalents, trigger, state register, decoder, graphic search, combinatorial problem.*

Statement of the problem. The dignity of codes converters (CC) by the method of equivalents accumulation as compared to other method is a high speed and the possibility of changing in the wide limits of ratio between speed and hardware costs.

The regulation of the ratio between speed and costs is achieved due to the choice of number of conversion steps (1, 2, 3, 4 or more) and by the choice of steps values, the variant of decomposition of the multi-bit CC into blocks, and also due to the use or serial or parallel strategy of the input counters reset in the multistage CC.

Analysis of recent research and publications. The performed researches on this subject are devoted to the system approach to designing of converters of codes [1-4], use of interfaces and mathematical models [5, 7], methodological bases of support of preservation of engineering works [6] and methods of visualization [8].

At the same time, insufficient attention is paid to various strategies for implementing code converters.

The purpose of this work is the analysis of the structure of CC functioning and formulation of the formation algorithm of the tables of laws functioning of the equivalents generator (EG) for CC with the different number of conversion steps:

– determination of lines' number of the EG, hardware costs of which are proportional to their number;
– comparative analysis of implementation methods of EG.

Presentation of the main research material

1. Serial strategy of usage of the conversion steps

Serial strategy of steps usage is implemented as a scheme more simply. Maximum number of conversion cycles of any K-ary input number into a binary code on an exit of CC for two-step (N_2), three-step (N_3) and three-step (N_4) CC is determined according to formulas (1):

$$\begin{gathered} N_2=](K\text{-}1)/a[+a\text{-}1; \\ N_3=](K\text{-}1)/b[+](b\text{-}1)/a[+a\text{-}1; \\ N_4=](K\text{-}1)/c[+](c\text{-}1)/b[+](b\text{-}1)/a[+a\text{-}1, \end{gathered} \tag{1}$$

where К – is a base of numeral system at the entrance; a – the second step of conversion (a > 1); b – the third step of conversion (a < b < c); c – the fourth step of conversion;] [– brackets mean round up to lowest integer. The first step is always equal to 1.

When serial strategy of the steps usage, the reset of the input counters is conducted with a most step [1].

Then, when all bits has a value that less than a biggest step, there is a transition to lowest step, and, on the last step, conversion is executed with a step 1.

For information reception about excess conversion step of the number X_i, triggers of state registers (table 1) and excess decoders (ED) are used.

Excess decoders are implemented on the base of combinational circuits. The condition of values formation of signals from the output of excess decoders is determined by expressions (2), (3), (4), (5).

Table 1.

Steps			
1	2	3	4
1	a	b	c
C_i	D_i	E_i	F_i

$$C_i=\begin{cases}1, X_i \ge 1;\\ 0, X_i = 0,\end{cases} \tag{2}$$

$$D_i=\begin{cases}1, X_i \ge a;\\ 0, X_i < a,\end{cases} \tag{3}$$

$$E_i=\begin{cases}1, X_i \ge b;\\ 0, X_i < b,\end{cases} \tag{4}$$

$$F_i=\begin{cases}1, X_i \ge c;\\ 0, X_i < c.\end{cases} \tag{5}$$

2. Parallel strategy of usage of the conversion steps

In the application of the parallel strategy of usage of the different conversion steps simultaneously in different bits can be used reduction of indicator of multi-bit counters on the value magnitude of the biggest from the steps of *c, b, a* or *1* (for the four-step CC) [2, 3]. Thus the value of the number

$$X_i(t+1) = X_i(t) - \gamma, \tag{6}$$

where $\gamma = \max\{c, b, a, 1\}$.

The application of the parallel strategy of usage of the different conversion steps decreases the maximal number of the conversion cycles in the two-step CC from 7 to 5, and in the three-step CC from 4 to 3.

To define the usage expediency of the parallel strategy, it is necessary to get the series of estimations of EG complexity for two strategies, and also formation algorithm of laws functioning of the EG [2]. Optimal values of conversion steps for parallel strategy it is possible to get by simulation (table 2) or using special software "Converter" [2]. In a table 2 *NT* means the number of the conversion cycle.

Table 2

NT	**К=12 Set of steps 1,4**
	11 10 9 8 7 6 5 4 3 2 1 0
1	7 6 5 4 3 2 1 0 2 1 0 0
2	3 2 1 0 2 1 0 0 1 0 0 0
3	2 1 0 0 1 0 0 0 0 0 0 0
4	1 0 0 0 0 0 0 0 0 0 0 0
5	0 0 0 0 0 0 0 0 0 0 0 0
NT	**К=12 Set of steps 1,2,5**
	11 10 9 8 7 6 5 4 3 2 1 0
1	6 5 4 3 2 1 0 2 1 0 0 0
2	1 0 2 1 0 0 0 0 0 0 0 0
3	0 0 0 0 0 0 0 0 0 0 0 0
4	0 0 0 0 0 0 0 0 0 0 0 0

For one-step EG at the number of bits of p = 2 we have a next table of EG (table 3). In a table 3 S means the general view of the equivalent.

Table 3

i	Step 1	S
	C_2 C_1	
0	0 0	0
1	0 1	$К^0$
2	1 0	$К^1$
3	1 1	$К^1 + К^0$

At the tables formation of laws of EG functioning for parallel strategy the full lexical-graphical search of all values of conversion steps (table 4 – table 6) is used.

Table 4

i	D_2 D_1	C_2 C_1	S
0	0 0	0 0	0
1	0 0	0 1	K^0
2	0 0	1 0	K^1
3	0 0	1 1	$K^0 + K^1$
4	0 1	0 1	$aK^0K^1 + aK^0$
5	0 1	1 1	
6	0 1	1 0	aK^1
7	1 0	1 1	$aK^1 + K^0$
8	1 0	1 1	$aK^0 + aK^1$

Table 5

i	D_2 D_1	C_2 C_1	S
0	0 0	0 0	0
1	0 0	0 1	K^0
2	0 0	1 0	K^1
3	0 0	1 1	$K^0 + K^1$
4	0 1	x 1	aK^0
5	1 0	1 x	aK^1
6	1 1	1 1	$aK^0 + aK^1$

From the analysis of table 3 it is necessary that in her overhead part for two-step CC 2^p combinations of junior group of variables are situated.

Then follows that for each combination of senior group with the number of ones j it is necessary to write down 2^{p-j} different combinations in junior group, which have p-j zeros, and having searched of all values of these bits we will get 2^{p-j} combinations with ones.

The number of all possible combinations with j ones in senior group equals to C_p^j.

Thus for two-step CC we will get the number of lines for EG by a formula (7).

$$N_2 = 2^p + \sum_{j=1}^{j=p-1} C_p^j \cdot 2^{p-j} + 1. \tag{7}$$

Table 6

i	E_2 E_1	D_2 D_1	C_2 C_1	S
0	0 0	0 0	0 0	0
1	0 0	0 0	0 1	K^0
2	0 0	0 0	1 0	K^1
3	0 0	0 0	1 1	$K^1 + K^0$
4	0 0	0 1	0 1	aK^0
5	0 0	0 1	1 1	$K^1 + aK^0$
6	0 0	1 0	1 0	aK^1
7	0 0	1 0	1 1	$aK^1 + K^0$
8	0 0	1 1	1 1	$aK^1 + K^0$
9	0 0	0 1	0 1	bK^0
10	0 1	0 1	1 1	$K^1 + bK^0$
11	0 1	1 1	1 1	$aK^1 + bK^0$
12	1 0	1 0	1 0	bK^1
13	1 0	1 0	1 1	$bK^1 + K^0$
14	1 0	1 1	1 1	$bK^1 + aK^0$
15	1 1	1 1	1 1	$bK^1 + bK^0$

In the study of the number of lines of EG tables for different number of bits the expression (7) we got:

$$N_m^{ФЭ} = (m+1)^p, \tag{8}$$

where m – number of different conversion steps .

The determination of number of lines of EG is a combinatory task. The number and values of coefficients C_p^j are determined by numbers of Paskal's triangle (table 7).

Table 7

p=0	1
p=1	1 1
p=2	1 2 1
p=3	1 3 3 1
p=4	1 4 6 4 1
p=5	1 5 10 10 5 1

The calculation results Nm для $\overline{m=1,4}$ and $\overline{p=1,5}$ are presented in Table 8.

Table 8

m	**p**				
	1	**2**	**3**	**4**	**5**
1	2	4	8	16	32
2	3	9	27	81	243
3	4	16	64	256	1024
4	5	25	125	625	3125
K_2	0,75	1,125	1,69	2,53	3,8
K_3	0,67	1,33	2,67	5,33	10,66
K_4	0,625	1,56	3,91	9,76	24,41

The schedule of winning (saving) the number of rows of the parallel EG compared to the method of direct selection of all combinations of EG in the parallel CC, respectively to a two-step, three-step, four-step CC is determined by formulas:

$$k_2 = \frac{N_m}{2 \cdot N_1} = \frac{N_2}{2 \cdot N_1} = \frac{3^p}{2 \cdot 2^p}; \tag{9}$$

$$k_3 = \frac{4^p}{3 \cdot 2^p}; \tag{10}$$

$$k_4 = \frac{5^p}{4 \cdot 2^p}. \tag{11}$$

A generalized formula for saving the number of rows of the parallel EG for any number of conversion steps m described by the expression (12):

$$k_i = \frac{N_m}{m \cdot N_1}. \tag{12}$$

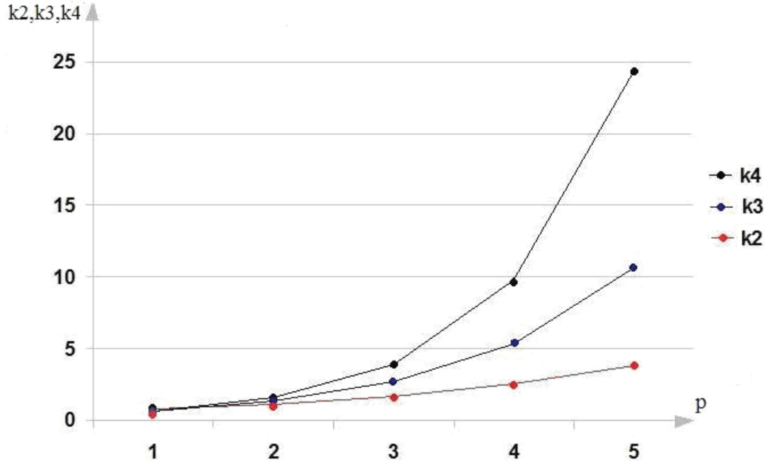

Figure 1. The schedule of changes k_2, k_3, k_4 in the function of the p bits of the EG

For two-step CC with different number of bits p (values of p are given in brackets) we have a system of formulas (13):

$$
\begin{gathered}
N_2(1) = 2^p + 1 \\
N_2(2) = 2^2 + C_2^1 \cdot 2^{2-1} + 1 = 2^2 + 2 \cdot 2 + 1 = 4 + 4 + 1 = 9 \\
N_2(3) = 2^3 + C_3^1 \cdot 2^{3-1} + C_3^2 \cdot 2^{3-2} + 1 = \\
= 2^3 + 3 \cdot 2^2 + 3 \cdot 2 + 1 = 8 + 12 + 6 + 1 = 27 \\
N_2(4) = 2^4 + C_4^1 \cdot 2^3 + C_4^2 \cdot 2^2 + C_4^3 \cdot 2 + 1 = 2^4 + 4 \cdot 2^3 + 6 \cdot 2^2 + 4 \cdot 2 + 1 = \\
= 16 + 32 + 24 + 8 + 1 = 81 \\
N_2(5) = 2^5 + C_5^1 \cdot 2^4 + C_5^2 \cdot 2^3 + C_5^3 \cdot 2^2 + C_5^4 \cdot 2 + 1 = \\
= 32 + 5 \cdot 2^4 + 10 \cdot 2^3 + 10 \cdot 2^2 + 5 \cdot 2 + 1 = 32 + 80 + 80 + 40 + 10 + 1 = 243.
\end{gathered}
\tag{13}
$$

The analysis of EG tables for other values of m shows that the number of lines $N_m^{\text{ФЭ}}$ is determined by the formula (14):

$$N_m = (m+1)^p ; m = 1, 2, ... \tag{14}$$

3. Formation algorithm of the tables of laws functioning of the EG

The analysis of the table 3 – table 6 allows formulating the following formation algorithm of the tables of laws functioning of the EG in the CC with parallel usage of the conversion steps:

We perform a complete searching (starting with zero combination) of all p-bit binary combinations of junior group of states' variables. While in the remaining m-1 senior groups (m – number of different conversion steps), all p bits of variables in each group becomes zero.

After receiving the one combination of variables of the group, where was searched, go to the searching of variables values of the neighboring senior group, excluding zero combination.

We determine the number of zeros in the regular combination of values of the variables of the current group. In the column of variables of the current group regular combination is repeated 2l times. In all p bits of variables of older groups relative to the current group it is necessary to write down the zero values, and in the bits, where variables of the current group have one values, in all the younger groups should also write ones, where were searched all different binary values (from 000 .... 0 to 111 ... 1) in 1 zero bits of the regular combination of the current group.

After receiving the unit combinations of variables of the current group it is necessary to compare the set of the current group j with the number of conversion steps m. If i < m, it is necessary to go to the searching of variables of the more senior group with number i + 1 (excluding the zero combination of variables). If i = m, then, go to the calculation of equivalents.

For receiving the decimal values of the j row equivalent of the table of laws functioning of the EG it is necessary to sum up the degree base k, that corresponding to one values of bits of the binary combinations of state variables of the current group, and then multiply the sum on the value of the conversion step, corresponding to the current group.

We perform the translation of the equivalent's decimal value to the binary number system.

We complete the formation of the table of laws functioning of the EG by specifying all source data: the base of the number system at the input, the number of bits at the input and output, number of conversion steps, values of the conversion steps and strategy of steps usage – parallel strategy.

Detailed system design of the multistep and multiblock code converters is performed by analyzing the hardware costs of the different decomposition variants of the multi-bit CC into blocks in accordance with the procedure [4].

Conclusions

The main results. The structure and operation of conversion codes by the method of equivalent accumulation are considered using a parallel strategy of using conversion steps, which, in comparison with a sequential strategy, allows reducing the number of conversion cycles from 7 to 5 (increasing the speed by 28%), and for a three-stage strategy - from 4 to 3 (increase speed by 25%).

The analytical expression for the number of rows in table of laws functioning of the EG in the CC with a parallel strategy of conversion steps usage in the function of radix on the inputs, the number of different conversion steps m and the number of variables p at the input of the EG, has been received.

We have analyzed two methods with a parallel strategy of using steps: a) based on the aggregation of decoders (DC), which distinguish all lines; b) on the basis of two decoders DC1 and DC2, which work separately, the lowest of which is controlled by the state of the flip-flops of the register of the highest states.

The practical significance is as follows. The conducted research allows one to accelerate the stage of system design of the CC with a parallel strategy of using steps; increase the speed of the spacecraft and reduce the hardware costs for building the main non-standard unit of the EG and the spacecraft as a whole.

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ПОРІВНЯННЯ МЕТОДІВ РЕАЛІЗАЦІЇ ФОРМУВАЧІВ ЕКВАВІВАЛЕНТІВ ПЕРЕТВОРЮВАЧАХ КОДІВ

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Розглянуто переваги перетворювачів кодів за методом накопичення еквівалентів у порівнянні з іншими елементами обчислювальних систем. Проведено аналіз двох способів реалізації формувача еквівалентів у перетворювачах коду, на основі тригерів регістрів стану та дешифраторів перевищення. Розглянуто та запропоновано алгоритм побудови таблиць законів функціонування основного нестандартного вузла у перетворювачах коду за методом накопичення еквівалентів. Отримані формули для визначення кількості рядків еквівалентів. Розглянуто паралельні та послідовні стратегії використання етапів трансформації. Проведено аналіз таблиць еквівалентних генераторів, для побудови яких використано лексико-графічне перерахування всіх етапів перетворення. Шляхом моделювання, а також з використанням спеціального програмного забезпечення «Converter», отримані оптимальні значення перетворення для паралельної стратегії. Сформульовано алгоритм побудови таблиць законів функціонування еквівалентних генераторів. Отримано аналітичний вираз для визначення кількості рядків у таблицях законів функціонування еквівалентних генераторів у перетворювачах коду з паралельною стратегією використання кроків перетворення. Створено передумови для розробки методики побудови таблиць формувача еквівалентів. Отриманий алгоритм побудови таблиць законів функціонування формувачів еквівалентів. Проведене дослідження дозволяє прискорити етап проектування перетворювачів кодів з паралельною стратегією використання кроків, що дасть змогу збільшити швидкодію обчислювальної системи і зменшити апаратурні витрати.

Ключові слова: *формувач еквівалента, перетворювач коду, алгоритм, аналіз, метод накопичення еквівалентів, тригер, регістр стану, декодер, графічний пошук, комбінаторна задача.*

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